WHAT IS CLAIMED IS:

1. In a process for manufacturing by chemical vapor deposition a tungsten-plug in a semiconductor device which comprises depositing a SiO_2 insulation layer on top of a substrate by CVD, then depositing a layer of BPSG onto the SiO_2 layer for surface planarization by employing CVD again; partially etching the SiO_2 layer and the BPSG layer to form a contact hole to the substrate; performing ion implantation through the contact hole and forming the device in the substrate; sputter depositing a barrier metal layer comprising a Ti and TiN bilayer in which the Ti metal is underneath the TiN in the Ti/TiN bilayer; wherein the improvement comprises depositing tungsten metal in two CVD chambers with different quartz clamp rings to control the area and thickness of the nucleation layer (50) and bulk deposition area of the tungsten layer (60) in order to ensure that the bulk deposition of tungsten is onto the nucleation layer; forming the tungsten-plug in the contact hole by a plasma anisotropic etch back procedure; and sputtering an Al/Si/Cu layer and pattern metal lines by conventional techniques.

2. A process for manufacturing a tungsten-plug avoiding volcano phenomena according to claim 1, wherein the said quartz clamp ring employed to form Ti and TiN by CVD is about 2mm wide.

3. A process for manufacturing a tungsten-plug avoiding volcano phenomena according to claim 1, wherein the quartz clamp ring employed to form tungsten nucleation layer by CVD is about 3mm wide.

4. A process for manufacturing tungsten-plug avoiding volcano phenomena according to claim 1, wherein the quartz clamp ring employed to form the bulk deposition of tungsten onto the tungsten nucleation layer is 5mm wide.

5. A process for manufacturing tungsten-plug avoiding volcano phenomena according to claim 1, wherein the tungsten nucleation layer deposited by CVD is about 500 angstroms thick.

6. In a process for manufacturing by chemical vapor deposition a tungsten-plug in a semiconductor device which comprises depositing a SiO_2 insulation layer on top of a substrate by CVD, then depositing a layer of BPSG onto the SiO_2 layer for surface planarization by employing CVD again; partially etching the SiO_2 layer and the BPSG layer to form contact holes to the substrate; making ion implantation through the contact holes and forming the device in the substrate; sputter depositing a barrier metal layer comprising Ti and TiN bilayer, in which the Ti metal is underneath the TiN in the Ti/TiN bilayer; wherein the improvement comprises depositing tungsten metal while holding the BPSG coated wafer in place with a first quartz ring having a diameter to form a first band and sputter depositing a barrier metal layer made up of Ti and TiN, onto the exposed BPSG layer in which the Ti metal is underneath the TiN layer, said barrier layer is not formed in the band width of said first ring band;

forming a tungsten nucleation layer on the wafer in one chemical vapor deposition chamber using a clamp quartz ring with a second diameter and a second band width which covers the first band and a small portion of the TiN/Ti barrier layer, by reacting WF_6 with SiH_4 to form a nucleation layer except in the band covered by said first and second quartz rings; transferring the thus treated wafer to a second vapor deposition chamber in which a third clamp ring is employed, said third clamp having a third diameter and third band width which covers the first and second band widths and a small portion of the wafer having the tungsten nucleation layer; forming a bulk tungsten layer in the second chamber by the reaction of WF_6 with H_2 to produce the bulk deposition of W onto tungsten nucleation layer of the wafer to cover contact holes;

forming the tungsten-plug in the contact hole by plasma anisotropic etchback technique.

7. The process of claim 6, wherein the quartz clamp ring employed during the formation of Ti and TiN by CVD is about 2mm wide.

8. The process of claim 6, wherein the quartz clamp ring employed to form tungsten nucleation layer by CVD is about 3mm wide.

9. The process of claim 6, wherein the quartz clamp ring employed to form the bulk deposition of tungsten onto the tungsten nucleation layer is 5mm wide.

10. The process of claim 6, wherein the tungsten nucleation layer deposited is about 500 angstroms thick.

11. A process for making a tungsten-plug in an integrated circuit device which comprises the steps of :

(1) Depositing a SiO_2 insulation layer (25) on top of a substrate (20) by CVD; and then depositing a layer of BPSG (30) onto the SiO_2 layer (20) for surface planarization by again employing CVD;

(2) Partially etching the SiO_2 insulation layer (25) and the BPSG layer (30) to form contact holes on the substrate (20);

(3) Making ion implantation through the contact hole and forming the devices;

(4) Sputter depositing a barrier metal layer made up of Ti followed by rapid thermal nitridation to form a TiN layer in which the Ti metal is underneath the TiN layer which is bilayer (40);

(5) Depositing tungsten (W) metal in two CVD chambers with different quartz clamp rings to control the area and thickness of the tungsten nucleation layer (50) and bulk deposition area of the tungsten (W) layer (60) in order to ensure the bulk deposition is onto the nucleation layer;

(6) Forming the tungsten-plug in the contact hole by plasma anisotropic

etch back technique;

(7) Sputtering on a Al/Si/Cu layer and pattern metal lines by conventional technology.

12. The process of claim 11, wherein the rapid thermal nitridation of step (4) takes place at about 760°C for about 30 seconds.